Top level timing and physical verification

Updated 20 03 2013
Functional verification of blocks

Analog blocks with Spectre based test benches
- Peer revision of schematic used for LVS
  - Ensure connectivity
  - Ensure intended functionality across all corners

Digital blocks
- Peer revision of netlist/schematic used for LVS
- Gate level testbenches including time annotation of delays, combining min/max delays for interconnected blocks
- Direct testing of all intended functionalities at block level
- Testing with random stimuli (if appropriate)
- Systematic revision of synthesis and P&R logs for ERRORS and WARNINGS
Top level interfaces, SI, Timing

Block interfaces
- A/A, A/D, D/D
  - Check compatibility of levels including GND/VDD rail voltage tolerances

Signal integrity
- Driving strength specified and rise time / fall time checked for all drivers
- Cross-talk evaluation \((NOT\ an\ option,\ only\ digital\ tools\ SI)\)

Timing
- Static Timing Analysis reports
  - Review interconnects that are not covered by STA \(TODO\ (SB,\ GAR,\ AK)\)
- Clock reports
  - Buffering should be where needed and only where needed
  - Clock networks skews \(TO\ CHECK\ (SB)\)
- Dynamic timing checks
  - SDF annotated gate-level simulation / analog testbenches
  - Cross-combine min/max models (voltage/process on-chip variations)
Power integrity

- DC IR drop rail analysis
  - Review and sign-off block level and chip level IR drops
    - Analog **OK** (Jan), Digital **OK** (GL), TDC **OK** (GL)
    - Check powering of dll_fanout TO DO (SB, MN)
  - Review effects of rail voltage tolerances on DAC/ADCs/References/Current Generator TO DO (JK)

- AC IR drop rail analysis
  - Drivers of large loads in each block to be considered for dynamic IR drops (ex. Serializers to Qchip intfc or signals to test pads)
  - Large clock trees properly decoupled
  - Review decoupling

- I/O pads powering
  - Currents in pads and bonds? ESD?
  - Coupling of power domains, any effects?
    - CLK_DLL input pads powered from SLVS
Top level sign-off

DFM / DFR

- Multi-cut vias
- Sections 5.3 and 5.4 (FEOL and BEOL Reliability rules)
  - Decoupling capacitors with thin oxide
    - Difficult to evaluate; impact on yield can be expected according to manual; option: remaster DECAP_SB cells with thick oxide versions, acceptable worsening of decap, potential significant impact on yield. GAR20130320
  - Maximum DC and AC current densities (electro-migration)

DRC / LVS / Chip edge

Chip design check list

- Query for sign-off checklist from GBT and FEI4 designs
- Matching sensor layout / pad-pitch / boundary tolerances (AK / JK)
- Meeting wire-bonding specs/constraints
- Section 1.7 IBM Manual “Chip design check list”
  - Latch-up rules ( JK, SB )
  - Well and substrate rules ( JK, SB )
  - Electro-static Discharge (ESD) and latchup layout and design requirements shall be met (see Section 3.10, “Latchup Rules” on page 176 and Section 3.11, “External Latchup Rules” on page 184 and Section 7.0 “Electrostatic Discharge (ESD)” on page 523)
- Appendix J.0 (Analog), Appendix L.0 (Design hierarchy)