Versatile Link PLUS
Transceiver Development

Csaba SOOS
EP-ESE-BE

on behalf of the VL+ collaboration
Outline

- Versatile Link **PLUS** project introduction
  - Key differences between VL and VL+
  - Link architecture, work packages
- VL+ front-end module
  - Variants
- Commercial module customisation
  - Customisation roadmap
- Custom module development
  - Prototype test results
- Summary
Introduction to Versatile Link PLUS

- The Versatile Link PLUS project (VL+) targets the phase II upgrades of the ATLAS and CMS experiments.
- VL+ was officially announced at ACES 2014 and started on 1 Apr 2014. It is subdivided in three phases of 18 months each:
  - Phase 1: proof of concept (Apr 2014 – Oct 2015)
  - Phase 2: feasibility demonstration (Oct 2015 – Apr 2017)
  - Phase 3: pre-production readiness (Apr 2017 – Oct 2018)
- Collaboration between CERN, FNAL, Oxford, and SMU

<table>
<thead>
<tr>
<th>Versatile Link</th>
<th>Versatile Link PLUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical mode</td>
<td>Single- and multi-mode</td>
</tr>
<tr>
<td>Flavours</td>
<td>Multi-mode</td>
</tr>
<tr>
<td>1Tx+1Rx, 2Tx</td>
<td>Configurable at build time up to nTx(+1Rx)</td>
</tr>
<tr>
<td>Radiation level</td>
<td>Calorimeter grade</td>
</tr>
<tr>
<td>Tracker grade</td>
<td></td>
</tr>
<tr>
<td>Form factor</td>
<td>SFP+</td>
</tr>
<tr>
<td>Custom miniature</td>
<td></td>
</tr>
<tr>
<td>Data rate</td>
<td>Tx/Rx: 5 Gb/s</td>
</tr>
<tr>
<td></td>
<td>Tx: 5/10 Gb/s, Rx: 2.5 Gb/s</td>
</tr>
</tbody>
</table>

Table: Key differences between VL and VL+
Versatile Link PLUS architecture

**Versatile Link PLUS**

![Diagram of Versatile Link PLUS architecture](image)

**On-Detector**
Custom Electronics & Packaging
Radiation Hard

**Off-Detector**
Commercial Off-The-Shelf (COTS)
Custom Protocol
VL+ project work packages

Reliability (Oxford, Academia Sinica)

Commercial Array TRx (FNAL)

Connectors, Fibres (CERN-EN)

Laser Driver (SMU)
Fibre plant – an example

Design of the passive optical cabling system

Cabling Scheme of CMS optical link from Front-end to Back-end

- MT Spring Clip
- Patch cable 24F (M03)
- Multi-fibre patch cable 144F (M05)
- MT to MTP adapter

MTP 24F connector
($L_{\text{max}} = 0.35 \text{ dB}$)

Counting Room

06 Mar. 2017

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VL+ front-end module

- Versatile
  - Up to 4Tx + up to 1 Rx, configurable at build time or by masking channels
  - 4Tx + 4Tx may become feasible (TBD)
- MM only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturised
  - Target dimensions 20 x 10 x <4 mm
  - Target dimensions 20 x 10 x 2.5 mm
- Pluggable
  - Either optical or electrical (or both) connector
  - No optical connector for lowest profile
- Data-rate:
  - Tx: 5 and 10 Gb/s
  - Rx: 2.5 Gb/s (and 5 Gb/s?)
- Environment
  - Temperature: -35 to + 60 °C
  - Radiation (based on Tracker requirements, TBD)
    - Total Dose: 1 MGy qualification (investigations up to 2 MGy)
    - Total Fluence: $1 \times 10^{15}$ n/cm$^2$ and $1 \times 10^{15}$ hadrons/cm$^2$

Total quantity 20k – 50k modules
**VL+ front-end module variants**

**Discrete-based**
derived from:
• Light peak
• USB-3
• Thunderbolt

1 TX + 1 RX

3 TX (single channel LDDs) + 1 RX

4 TX (single channel LDDs)

**Array-based**
derived from:
• QSFP+ engine
• Mid-Board engine

1/3/4 TX (using LDD array) + 1 RX

4/8 TX (using LDD arrays)
Dual approach

- Modification of existing commercial modules
  - Working in close collaboration with various industrial partners
    - Minimise customisation to retain cost benefit from volume production

- In-house design of module
  - Working in close collaboration with suppliers of optical coupling blocks
  - Working in close collaboration with industrial partner on integration
    - CERN-designed PCB
    - CERN-specified or procured opto-die
    - CERN-specified or procured ASICs (LDD, TIA-LA)
  - Potentially the path to highest level of affordable customisation
Customisation steps

- Progression from standard component to full-custom object suitable for CERN project needs
  - Start with evaluation of standard component and sub-components (Steps 0/1) on a per-vendor basis

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Commercial roadmap

- Development (*until 2018*)
  - CERN Market Survey
    - CERN issues Technical Requirement & Questionnaire
    - Companies return completed Questionnaire
    - CERN reserves the right to order samples (Steps 0, 1) and/or ASIC drop-ins to existing parts for evaluation (Steps 2, 3)
    - CERN qualifies companies having required technology
  - CERN Price Enquiry
    - Qualified companies receive full technical specification for development
    - Qualified companies bid for development (Step 4)

- Production (*2019-20 onwards*)
  - Companies having successfully completed development (on time, in budget) will be invited to tender for full production
  - One or two lowest cost bidder(s) will receive production contract
### Custom VL+ front-end prototypes

In-house design and development of full custom module

<table>
<thead>
<tr>
<th>Version</th>
<th>V1</th>
<th>V2</th>
<th>V3 and V3b</th>
<th>V4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Config.</td>
<td>1Tx + 1Rx</td>
<td>1Tx + 1Rx</td>
<td>4Tx + 1Rx</td>
<td>2Tx + 1Rx</td>
</tr>
<tr>
<td>Optical I/F</td>
<td>US conec MOI</td>
<td>Low-profile</td>
<td>US conec MOI</td>
<td>Low-profile</td>
</tr>
<tr>
<td>Electrical I/F</td>
<td>SFP</td>
<td>SFP</td>
<td>QSFP</td>
<td>Custom</td>
</tr>
<tr>
<td>Receiver</td>
<td>GBTIA + ULM PIN</td>
<td>GBTIA + ULM PIN</td>
<td>GBTIA + ULM PIN</td>
<td>GBTIA + ULM PIN</td>
</tr>
<tr>
<td>Transmitter</td>
<td>COTS driver + ULM VCSEL</td>
<td>COTS driver + ULM VCSEL</td>
<td>LDQ10/LDQ10P + VCSEL array</td>
<td>LDQ10Pv2 + VCSEL array</td>
</tr>
</tbody>
</table>
Custom module development roadmap

Legend:
MOI – Mechanical Optical Interface
GBTIA – CERN receiver ASIC
GBLD10+ – CERN single-channel VCSEL driver ASIC
LDD array – 4-channel Laser Diode Driver array
V3 prototype – TX performance

Device 7, TX1 @ 10 Gb/s

Device 7, TX2 @ 10 Gb/s

Device 7, TX3 @ 10 Gb/s

Device 7, TX4 @ 10 Gb/s

Device 7 TX eye parameters at 10 Gb/s
Device 7, using a reference SFP+ as transmitter at 4.8 Gb/s PRBS-7
Summary

- We made a lot of progress in the 2\textsuperscript{nd} phase of the Versatile Link PLUS project
- Market survey has been completed. Firms willing to work with CERN on transceiver customisation have been identified
- Price Enquiry for development costs to be issued by mid-2017
- CERN’s full custom development
  - 4 prototypes have been designed by CERN and 3 have already been manufactured by an industrial partner
- Functional tests carried out in the laboratory prove the good performance of the assembled prototypes