The Gigabit Link Interface Board (GLIB) specifications

v1.7

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Document History

- v1.7, 2010.09.03: Fig.A-2 and Sections §5.2 are modified.
- v1.6, 2010.09.01: All figures of Chapter 1 and Appendix A are modified. Fig.3-2 & Fig.3-9 are modified. The text of Example1 in Appendix A is modified.
- v1.5, 2010.08.20: Section §2.5, Fig.3-2, Fig.3-3, Section §3.5, Fig.3-10, Fig.3-11, Fig.4-2 and Appendices A & B are modified.
- v1.4, 2010.08.13: Chapter1, Sections §2.2, §3.1, §3.2, §3.6, §3.7, §3.8, Chapter 4 and Appendices A & B are modified. Chapter “Functional” is added. The numbering scheme of figures and tables has changed.
- v1.3, 2010.05.31: Colours of Fig.2, 15 & 16 changed. Minor correction in Fig.12. §2.5 modified. References changed accordingly.
- v1.2, 2010.05.12: The “Powering” section is slightly modified. Chapter 3 renamed to “Electrical”. The order of the sections in Chapter 3 is changed. Examples of typical GLIB use are added. Ambiguous sentences rephrased in few locations.
- v1.1, 2010.05.06: The XC2C64A CPLD is replaced by a XC2C128 that has more I/O pins. A preliminary list of the major components is added in Appendix B. §3.3 text, Fig.5 and §3.4 text are modified. Text is added in §3.1. The “Configuration and Testability” chapter is moved under Chapter 3 (as §3.8) and its text and associated Fig.12 are modified. Chapters “Mechanical” and “References” are now Chapter 4 and 5, respectively. Typos corrected in several locations.
- v1.0, 2010.05.04: Figures 3, 4 and 12 of v0.9 modified. Chapter 4 renamed to “Configuration and Testability” and expanded accordingly. Section “Module Management” added. Section “Examples of the GLIB use” moved to Appendices. SRAM type mentioned in §2.3.
- v0.9, 2010.04.28: Introduction has been added. Figures have been numbered. Page numbers have been added in the table of contents.
- v0.8, 2010.04.23: The QSFP and the 1x2 SFP+ cage are replaced with a 1x4 SFP+ cage while four transceiver lines are now routed to the primary FMC. All related text as well as the architecture, clock distribution and floor-planning figures have been changed accordingly. Ambiguous sentences rephrased in several locations. The voltages used are now explicitly mentioned in §3.3. An “optical interface extension” mezzanine has been added in the list of FMCs.
- v0.7, 2010.04.22: first draft in the document history.
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1. INTRODUCTION

The Gigabit Link Interface Board (GLIB) is an evaluation platform and an easy entry point for users of high speed optical links in high energy physics experiments. Its intended use ranges from optical link evaluation in the laboratory, to control triggering and data acquisition from remote modules in beam or irradiation tests. The GLIB is a double width Advanced Mezzanine Card (AMC) conceived to serve a small and simple system residing either inside a μTCA crate or on a bench with an optional serial link to a PC.

Each GLIB card can process data to/from four SFP+ transceiver modules, each operating at bi-directional data rates of up to 6.5 Gbps. This performance matches comfortably the specifications of the GBT/Versatile Link project [1] with its targeted data rate of 4.8 Gbps. In its simplest form, one GLIB board thus interfaces with up to four GBT channels.

Fig. 1-1 highlights the baseline configuration of a GBT-Versatile Link-GLIB system, where the GLIB converts data to/from the optical domain, implements the GBT protocol and codes/decodes the user payload at the link back-end.

The GLIB I/O capability can be further enhanced with two FPGA Mezzanine Cards (FMCs). This gives users the flexibility to adapt the GLIB interface to their system, by for instance adding connectivity to the TTC network at the backend, or connecting to e-links at the frontend. Fig. 1-2 illustrates a case where two GLIB boards are interconnected back-to-back, allowing implementing and experimenting with GBT-based systems well before full-fledged GBT ASICs become available.

Fig. 1-1: The GLIB board in a GBT-Versatile Link system

Fig. 1-2: Back-to-back interconnected GLIB boards with customization mezzanines (TTC and E-Link) drawn in yellow.
2. FEATURES

2.1. Overview

- General purpose double width AMC module for µTCA environment or bench-top use.
- Based on a high-performance Virtex-6 FPGA with 6.5Gbps transceivers.
- Up to four optical transceiver links on-board.
- Sockets for two expansion FMCs for user-specific I/Os and up to four additional 6.5Gbps transceiver lines (optional).

2.2. Interfaces

**Optical**

- Four cages for up to four hot-pluggable single-channel SFP+ transceiver modules (rated at 10Gbps) compatible with the GBT/versatile link.

**AMC**

- Port [0-1]: GbE.
- Port [4-7] (Fat Pipe): PCIe x4 GEN2. Possibility to implement other protocols.
- Port [8-11] (Extended Fat Pipe): PCIe x4 GEN2. Possibility to implement other protocols.
- Port [2:3]: LVDS I/O pairs. Possibility for implementing other differential I/O standards.
- Port [12-15]: LVDS I/O pairs. Possibility for implementing other differential I/O standards.
- Port [17-20]: M-LVDS.
- CLK1/TCLKA: M-LVDS clock input.
- CLK2/TCLKB: M-LVDS clock input/output.
- CLK3/FCLKA: HCSL/M-LVDS clock input.

**FMC**

- High-pin count (HPC) sockets rated at 18Gbps [2] for hosting up to two FMC mezzanines.
- Each HPC socket provides up to 160 user-specific I/Os (that can be configured both as single-ended or differential pairs) as well as 2 differential clock inputs and 2 differential clock outputs. The maximum targeted data rate is 500Mbps per single-ended I/O and 1Gbps per differential pair I/O.
- One FMC (referred-to as primary or FMC#1) is accessible from the front panel while the other one (referred-to as secondary or FMC#2) is accessible from the rear.
- The primary FMC also provides four optional 6.5Gbps transceiver lines. No components will be placed under it to allow the use of optical transceiver modules that violate the FMC specification’s maximum I/O depth of 31mm.

**PC (only in bench-top operation)**

- GbE RJ45 socket (1000BASE-T).
- PCIe 4x GEN2 adapter board.
- Possibility to implement additional PC interfaces on the FMC mezzanines.
2.3. On-board memory

- Two 72Mb (2M x 36bit) SRAM devices (CY7C1470 by Cypress) operating at up to 250MHz.

2.4. FPGA

- FPGA family: XILINX Virtex-6 LXT.
- FPGA device: VLX130T-1FF(G)1156C
  - 600 I/O that can be configured to various differential or single-ended standards.
  - Single-ended I/O data rates of up to 800Mbps.
  - 4 Ethernet MAC and 2 PCIe Hard-IP blocks.
  - 20 6.5Gbps transceivers (MGTs) organized in 5 quads.
    - One MGT quad for the SFP+ modules.
    - One MGT quad for the optional FMC#1 transceivers.
    - One MGT quad for the AMC Port [4:7].
    - One MGT quad for the AMC Port [8:11].
    - One MGT quad for the AMC Port [0:1].
  - ~10Mb of block RAM.
  - More than 50% of the total FPGA logic resources available for user logic.

2.5. Module Management Controller (MMC)

- Mezzanine card based on an ATMEL ATmega64/128 microcontroller.

2.6. Expansion/Upgradeability

- The system I/Os can be customized via FMC mezzanines.

- Possibility to use one of the following pin-to-pin compatible FPGAs:
  - VLX195 (~50% more logic resources, ~12Mb block RAM)
  - VLX240 (~85% more logic resources, ~14Mb block RAM)
  - VLX365 (~180% more logic resources, ~14Mb block RAM)
  - VSX315 (~140% more logic resources, ~25Mb block RAM)

- Possibility to use up to 1.125Gb SRAM devices once available.
3. ELECTRICAL

3.1. Architecture

Fig. 3-1 illustrates a block diagram of the GLIB architecture, where all major interconnections are shown.

- The clock distribution circuitry is presented in §3.2.
- The module management features are mentioned in §3.3.
- The JTAG circuitry is shown in §3.4.
- Various uses of the FMC sockets are proposed in §3.5.
- Some details concerning the powering of the system are provided in §3.6.
- The requirements of the μTCA environment are mentioned in §3.7 and §3.8.

![Fig. 3-1: Block diagram of the GLIB AMC card.](image-url)
### 3.2. Clock distribution

![Clock Distribution Diagram](image)

**Fig. 3-2:** The clock distribution scheme.

- When the reference clocks of MGT quads are driven through the AMC edge connector, the use of jitter attenuators is strongly recommended by the FPGA vendor.
- The use of external clock multipliers is required in case the reference clocks of the MGTs are below 100MHz.
- The use of the external clock multipliers gives flexibility in the configuration of the MGTs, since depending on the preferred communication protocol different reference clocks are often required.
- A dedicated clock jitter attenuator is also used for PCIe applications.
- Each MGT Reference clock (REFCLK) can be used to clock its neighbouring MGTs (e.g. the MGT114 REFCLK0 can also clock the MGT quads 113 and 115. Details about the Virtex-6 clocking resources can be found in [3].
- An option to operate the GLIB by using a crystal oscillator or an external clock source is foreseen for more user flexibility (the default frequency is 40MHz).
3.3. Module Management

- IPMI interface, geographical addressing and automatic module detection support.
- Hot swap support (by checking the state of the front Panel’s module handle switch).
- Control of the front panel LEDs according to the specification.
- Monitoring of the on-board temperature and voltage regulation.
- Communication with CPLD and FPGA through I2C and I/O.

![Module Management Controller circuitry.](image)

3.4. Configuration and Testability

- The JTAG circuitry supports both device configuration and Boundary Scan testing.
- The JTAG circuitry is based on a XC2C128 Coolrunner-II CPLD with 80 I/O that is used as JTAG switch in order to provide various JTAG chain options.
- The device configuration options provided are:
  - Configuration of FPGA and FPGA EEPROM: by the JTAG header#2 or the AMC edge connector JTAG or the AMC edge connector I2C (through MMC). Additionally, the FPGA EEPROM can be configured by the AMC Port [0] or Port [1] (through FPGA). Note that the FPGA EEPROM will have two pages in order to allow reverting to a previous working FPGA firmware (in case of failure).
  - Configuration of MMC: by the JTAG header#2 or the AMC edge connector JTAG.
  - Configuration of CPLD: by the JTAG header#1 (for safety reasons).
- For testability reasons, all other ICs on-board supporting Boundary Scan testing are chained and connected to the JTAG switch. The Boundary Scan testing procedure is to be defined.
3.5. Mezzanine cards

The GLIB AMC card FMC connectors are of type Samtec SEAF-40-S-06.5-10-A. The mating connectors of the FMCs are of type Samtec SEAM-40-S-03.5-10-A for 10mm stacking height or Samtec SEAM-40-S-06.5-10-A for 13mm stacking height.

Typical FMC functionalities could be:

- “TTC mezzanine”, for timing/trigger/clocking signals distribution (see Fig.3-5).
- “High density E-Link Mezzanine”, with two VHDCI connectors, each carrying 11 E-Links (see Fig.3-6).
- “Low density E-Link Mezzanine”, with four HDMI connectors, each carrying 1 E-Link (see Fig.3-7).
- “GBTX Parallel Bus mezzanine”, providing access to the 40+40bits of the GBTX parallel bus (see Fig.3-8).
- “USB3.0 mezzanine”, for high-speed connection to PC (see Fig.3-9).
- “Optical interface extension mezzanines” equipped with SFP+, QSFP, partially connected SNAP12, XPAK or other optical module types (see Fig.3-10), in order to take advantage of the four additional 6.5Gbps transceiver lines provided by the primary FMC socket. Various protocols could be implemented (e.g. 10GbE).
Fig. 3-5: Block diagram of the TTC FMC.

Fig. 3-6: Block diagram of the High Density E-Link FMC.

Fig. 3-7: Block diagram of the Low Density E-Link FMC.
Fig. 3-8: Block diagram of the GBTX Parallel Bus FMC.

Fig. 3-9: Block diagram of the USB3.0 FMC.

Fig. 3-10: Block diagram of an optical interface extension FMC.
3.6. Powering

- The 3.3V management power (MP) provided by the AMC edge connector is used for the powering of the MMC and the CPLD while the 12V payload power (PWR) is used for the powering of all other components. Additionally, a connector for powering the GLIB in bench-top operation is also available.

- The powering scheme incorporating the LT3021 and MAX8556 linear regulators, the LTM4601 and LTM4606 switching regulators and the LTC6902 multi-phase oscillator is shown in Fig.3-11.

![Fig.3-11: The powering scheme.](image)

3.7. MCH requirements

- GbE interface on MCH Fabric[A].
- Fabric clock to the MCH CLK3 (and/or MCH CLK1).
- Ability to receive the MCH CLK2 (driven by an AMC card) and forward it to MCH CLK1 and/or MCH CLK3.
- Ability to receive clock from External CLK input and forward it to the MCH CLK1 and/or MCH CLK3.
- Note that the selection of the appropriate MCH Fabric[D:G] depends on the configuration of Port[4:7] and Port[8-11].
3.8. Backplane requirements

No special requirements for the backplane.

- For a non-redundant backplane architecture:
  - MCH 1 Fabric[A] routed to AMC Port[0] for all μTCA slots.
  - The MCH CLK1 and CLK3 drive the AMC [1:12] CLK1/TCLKA and CLK3/FCLKA, respectively, while the MCH receives the AMC CLK2/TCLKB from all μTCA slots.

- For a redundant backplane architecture:
  - MCH 1 Fabric[A] routed to AMC Port[0] for all μTCA slots.
  - The MCH1 CLK1 drives the AMC[1:6] CLK1/TCLKA and the MCH2 CLK1 drives the AMC[7:12] CLK3/FCLKA, while the MCH1 and MCH2 receive the AMC CLK2/TCLKB from all μTCA slots.

- GLIB is compatible with the μTCA Physics backplane.
4. MECHANICAL

- Double width, mid- or full- size AMC module (depending on configuration). Extended card-edge interface (two-sided, 170-pin).
- The PCB dimensions are shown in Fig.4-1 (Component Side2 view).
- The floor-planning of the Component Side1 is shown in Fig.4-2.
- All remaining components not shown in the floor-planning of Component Side1 (e.g. the clock distribution circuitry) are accommodated in Component Side2 since they are low-profile. The floor-planning of the Component Side2 is to be defined.

Fig.4-1: Double width AMC module PCB dimensions, Component Side 2 (bottom) view [4].
Fig. 4-2: The GLIB floor planning, Component Side 1 (top) view.
5. FUNCTIONAL

5.1. Firmware Architecture

Fig. 5-1 shows the GLIB FPGA firmware architecture. The principle components are:

- The GbE interface (UDP protocol will be used).
- The Fat Pipe interfaces. Different flavors will be implemented.
- The external SRAM interface.
- The controller of the clock distribution circuit.
- The interfaces to the FMC mezzanines. Different flavors will be implemented depending on the hardware.
- A general purpose pattern generator.
- The GBT IP [5].
- The user logic block. This contains the treatment of the GBT payload, and differs depending on the application.

As shown in Fig. 5-1, most of the firmware blocks are attached to the FPGA local bus. The FPGA local bus is controlled either by the GbE or the Fat Pipe interface (depends on the user logic implementation).

All firmware blocks illustrated will be provided and supported by the GLIB team, except of the user logic and the GBT IP blocks. However, few implementation examples including the user logic and the GBT IP blocks will also be provided.
5.2. Bandwidth Considerations

**PCIe**
- PCIe Transfer Rate: 2.5Gbps/lane for GEN1, 5.0Gbps/lane for GEN2 (per direction).
- PCIe Maximum Data Throughput (write) = 68.8% of PCIe Transfer Rate [6].
- PCIe Maximum Data Throughput (read) = 60.8% of PCIe Transfer Rate [6].
- GLIB PCIe links: Up to two PCIe x4 (GEN1 or GEN2).

**GbE**
- GbE Transfer Rate: 1.25Gbps (per direction).
- GbE Theoretical Bandwidth: 1.0Gbps.
- GbE Maximum Data Throughput: 800Mbps [7].

**GBT**
- GBT Transfer Rate: 4.8Gbps (per direction).
- GBT Data/TTC/EC throughput = 3.2Gbps.
- GBT Slow control throughput = 80Mbps.
- GBT control throughput = 80Mbps.
- GLIB GBT links: Up to four (plus up to additional four on the FMC#1).

**E-Link**
- 80Mbps or 160Mbps or 320Mbps (configurable) [10].
- GLIB E-Links: Up to 22 per FMC.

**Others**
- Max GBT Event Size (assuming 100KHz trigger rate)= 3.2Gbps/100KHz=32Kbit.
- GLIB Storage capacity (assuming Max Event Size) = 144Mbit/32Kbit=4500 events.
6. REFERENCES

[1] GBT / Versatile link project.


http://www.picmg.org/pdf/AMC.0_R2.0_Short_Form.pdf


http://indico.cern.ch/getFile.py/access?contribId=5&sessionId=1&resId=0&materialId=slides&c onfId=90024

http://indico.cern.ch/getFile.py/access?contribId=6&sessionId=1&resId=0&materialId=slides&c onfId=90024

[10] Paulo Moreira, “GBT specifications draft v1.2”
https://espace.cern.ch/GBT-Project/GBTX/Specifications/gbtxSpecsV1.2.pdf
APPENDIX A: TYPICAL GLIB USE CASES

EXAMPLE1: GLIB as Back-End system, bench-top mode.

The GLIB is operating in bench-top mode. An external power supply is used. For the reception of timing/trigger information, the GLIB is equipped with a TTC mezzanine. The GLIB communicates with the front-end via GBT links. In Fig.A-1, the configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through a GbE connection. The SRAM can be used for intermediate storage, if necessary. Fig.A-2 and Fig.A-3 show two different flavours of the GLIB as back-end system in bench-top operation. In Fig.A-2, the configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through the GLIB PCIe adapter. In Fig.A-3, the GLIB is equipped with an Optical Extension mezzanine providing a fast optical interface (e.g. 10GbE) for the transfer of the GBT payload.

Fig.A-1: Example of the GLIB as back-end system. Mode: bench-top. Payload interface: GbE.

Fig.A-2: Example of the GLIB as back-end system. Mode: bench-top. Payload interface: PCIe.
EXAMPLE2: GLIB interfacing directly with Front-End chips, bench-top mode.

The GLIB is operating in bench-top mode. An external power supply is used. For the reception of timing/trigger information, the GLIB is equipped with the TTC mezzanine. For the direct communication with the front-end chips (without the use of GBT), the GLIB is also equipped with an E-Link mezzanine. The configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through a GbE connection. The SRAM can be used for intermediate storage, if necessary.

Fig.A-4: Example of the GLIB interfacing directly with front-end chips. Mode: bench-top. Payload interface: GbE.
EXAMPLE3: GLIB as Back-End system, μTCA crate mode.
The GLIB is operating inside a μTCA crate. The crate management by the MCH is controlled through a GbE link. For the reception of timing/trigger information, the GLIB is equipped with the TTC mezzanine. The GLIB communicates with the front-end via GBT links. In Fig.A-5, the configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done by a GbE connection, through the MCH’s GbE switch. The SRAM can be used for intermediate storage, if necessary. Fig.A-6 shows a different flavour where configuration of the GLIB as well as the transfer of the GBT payload from/to an AMC CPU is done through the MCH’s PCIe switch. The AMC CPU stores the data to an AMC storage medium through a SATA link.

Fig.A-5: Example of the GLIB as back-end system. Mode: crate. Payload interface: GbE.
Fig. A-6: Example of the GLIB as back-end system. Mode: crate. Payload interface: PCIe.
### APPENDIX B: COMPONENTS LIST

Table B-1: Preliminary list of the major components

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Manufacturer</th>
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</thead>
<tbody>
<tr>
<td>XC6VLX130T-1FF1156C</td>
<td>Virtex-6 LXT series FPGA</td>
<td>XILINX</td>
</tr>
<tr>
<td>XCF128X-FTG64C</td>
<td>Platform Flash XL for Virtex-6</td>
<td>XILINX</td>
</tr>
<tr>
<td>XC2C128</td>
<td>Coolrunner II CPLD</td>
<td>XILINX</td>
</tr>
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<td>SEAF-40-S-06,5-10-A</td>
<td>FMC HPC connector, Female, 400-pin</td>
<td>SAMTEC</td>
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<tr>
<td>2007132-1</td>
<td>SFP+ 1X4 Ganged Cage Assembly without light pipe</td>
<td>TYCO</td>
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<tr>
<td>1888247-1</td>
<td>PT connector assembly, 20pos, 0.8mm pitch, for SFP+</td>
<td>TYCO</td>
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<td>LTM4601EV#PBF</td>
<td>Adj. Voltage 12A DC/DC μModule</td>
<td>Linear Technology</td>
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<tr>
<td>LTM4606EV#PBF</td>
<td>Adj. Voltage 6A Ultralow EMI DC/DC μModule</td>
<td>Linear Technology</td>
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<td>LTC6902</td>
<td>Multiphase Oscillator</td>
<td>Linear Technology</td>
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<td>MAX8556</td>
<td>4A Ultra-Low-Input-Voltage LDO Regulators</td>
<td>MAXIM</td>
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<td>LT3021</td>
<td>500mA, Low Voltage, Very Low Dropout Linear Regulator</td>
<td>Linear Technology</td>
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<td>IDT5V5216PGG</td>
<td>Type-1/Type-2 M-LVDS to LVDS Transceiver</td>
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<td>Micrel</td>
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<td>LVDS 4x4 Crosspoint Switch</td>
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<td>ICS874003-05</td>
<td>PCIe clock jitter attenuator</td>
<td>IDT</td>
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<tr>
<td>ICS555G-03</td>
<td>PCIe clock (100MHz or 125MHz)</td>
<td>IDT</td>
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<tr>
<td>CY7C1470</td>
<td>2Mx36 200MHz SRAM (upgradeable up to 32Mx72)</td>
<td>Cypress</td>
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